out-of-band energy while also minimally effecting in-band energy. The embodiment shown in Figure 3 implements spectral shaping with a digital filter. The analog filter serves to reject images of the digital processing. Another embodiment eliminates the digital transmit filter. In this case, the spectral shaping is provided by the analog filter.

The digital to analog converter 316 is generally understood to convert a digital signal to an analog signal. In the embodiment shown in Figure 3, the transmission on the line occurs in an analog format.

The analog filter 322 performs final filtering of the analog waveform to spectrally prepare the signal for transmission over the line 202. The analog filter 322 may operate similarly to the transmit filter 312 but in the analog domain.

In one embodiment of the scrambler 304, the scrambler is configured to generate periodic sequences having good autocorrelation properties. One example of a signal with good autocorrelation properties is a signal that can be made to closely approximate an impulse. As can be understood, an impulse is a signal that, within a very short interval of time, assumes a substantially non-zero value while being approximately zero outside this time interval. An impulse response characterizing the line/channel is one desirable outcome of channel analysis or for detection. It is contemplated that a device other than a scrambler may be configured to generate the periodic sequences used for line probing. Any device or configuration of hardware and/or software may be adopted for use for generating sequence signals without departing from the scope of the invention.

Figure 4 illustrates a block diagram of an example embodiment of a sequence generator configured using a linear feedback shift register or scrambler type implementation. An input 400 connects to a summing unit 404. All arithmetic operations may be performed in a modulo-2 fashion. The summing unit 404 has an output connected to an output line 408 and a delay register 410A. The output of the delay register 410A connects to a multiplier 414A, having a multiplier set to C_1, and to another delay register 410B. The output of delay register 410B connects to N number of other delay registers and multipliers until connecting to a delay register 410C and to a multiplier C_{N-1}. The output of delay register 410C connects to a multiplier 414C that has a multiplier C_N. This creates an Nth order generator due to the N memory elements or delay registers 410. This thus generates an output based on the content of the registers, also known as the state of the scrambler. Thus, the total number of different possible states of the generator is 2^N.

In one example method of operation, a continuous sequence of logic value 1's is provided to the input 400. The state of each register may be selectively loaded with a logical one or a logical zero based on the desired sequence to be generated. When provided with a string of logics one values, the generator outputs a unique string, or sequence, of 1's or 0's based on the values of the registers 410. In one embodiment, the values loaded into the registers are selected to form a primitive polynomial known to generate a maximal length sequence (M-sequence). The sequence will repeat through the 2^N-1 non-zero states.

Figure 5 illustrates an alternative embodiment of a sequence generator. The embodiment shown in Figure 5 comprises a tapped delay line configuration designed to generate a sequence for use with the systems described herein. As shown in Figure 5, an input 504 connects to a delay register 508 that is configured to receive and delay for a clock cycle or other period the received value. The input 504 also connects to a multiplier 512A having a multiplier value M_0. All arithmetic operations in this embodiment may be performed in the traditional fashion, that is, not modulo-2. The output of the multiplier 512A connects to a summing junction 524.

The output of the register 508 connects to multiplier 512B having a multiplier value M_1. The output of the multiplier 512B connects to the summing junction 524 to add the output of the multiplier 512B and the multiplier 512A. The output of the register 508 also connects to a register 516, the output of which connects to multiplier 512C. The output of the multiplier 512C connects to summing junction 536, which also receives the output of summing junction 524. The tap delayed line 500 continues in this configuration until connecting to a register 532 that has an output connected to a multiplier 512D with a multiplier factor $M_2{}^N{}_{-1}$. The output of multiplier 512D connects to a summing junction 544 that also receives the output of the previous summing junction.

This configuration is 2^N-1 long with the elements of the tapped delay line controlling the sequence generated. Specifically, the coefficients of the tapped delay line are the sample values of the desired sequence signal. An input of a pulse followed by zero-valued samples to the tapped delay line propagates through the tapped delay line and